

**A 1GHz 192.389 fJ
6-bit Absolute-Value Detector**

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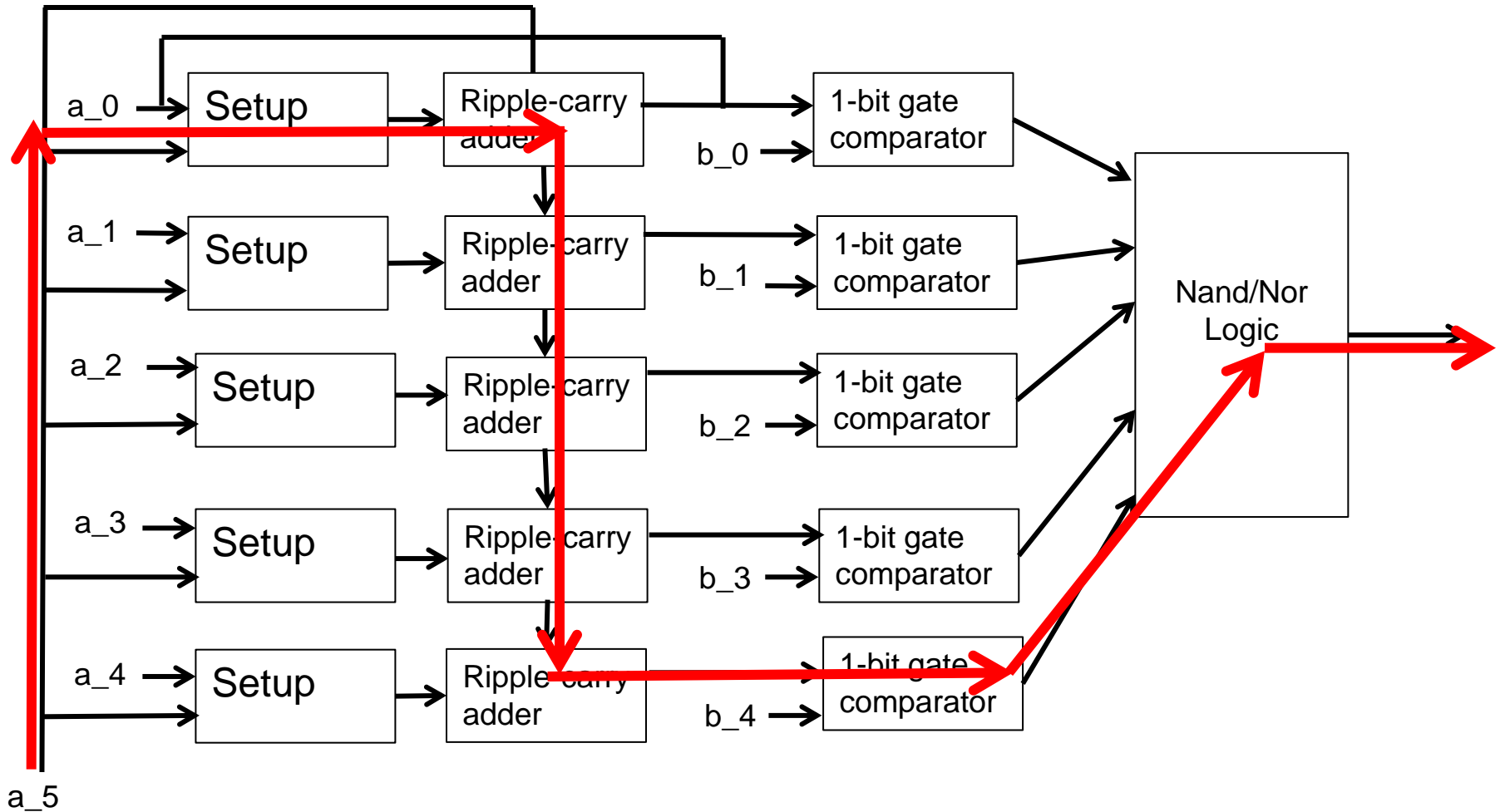


Design Summary

- ◆ A) Circuit topology – Ripple Carry Adder + Nand-Nor Comparator
- ◆ B) Circuit Style – Static CMOS and transmission gate XOR's
- ◆ C) WHY: Simplicity of Design, fast, moderate area, minimizes transistors, only sizes 2 gates for optimal fan-out

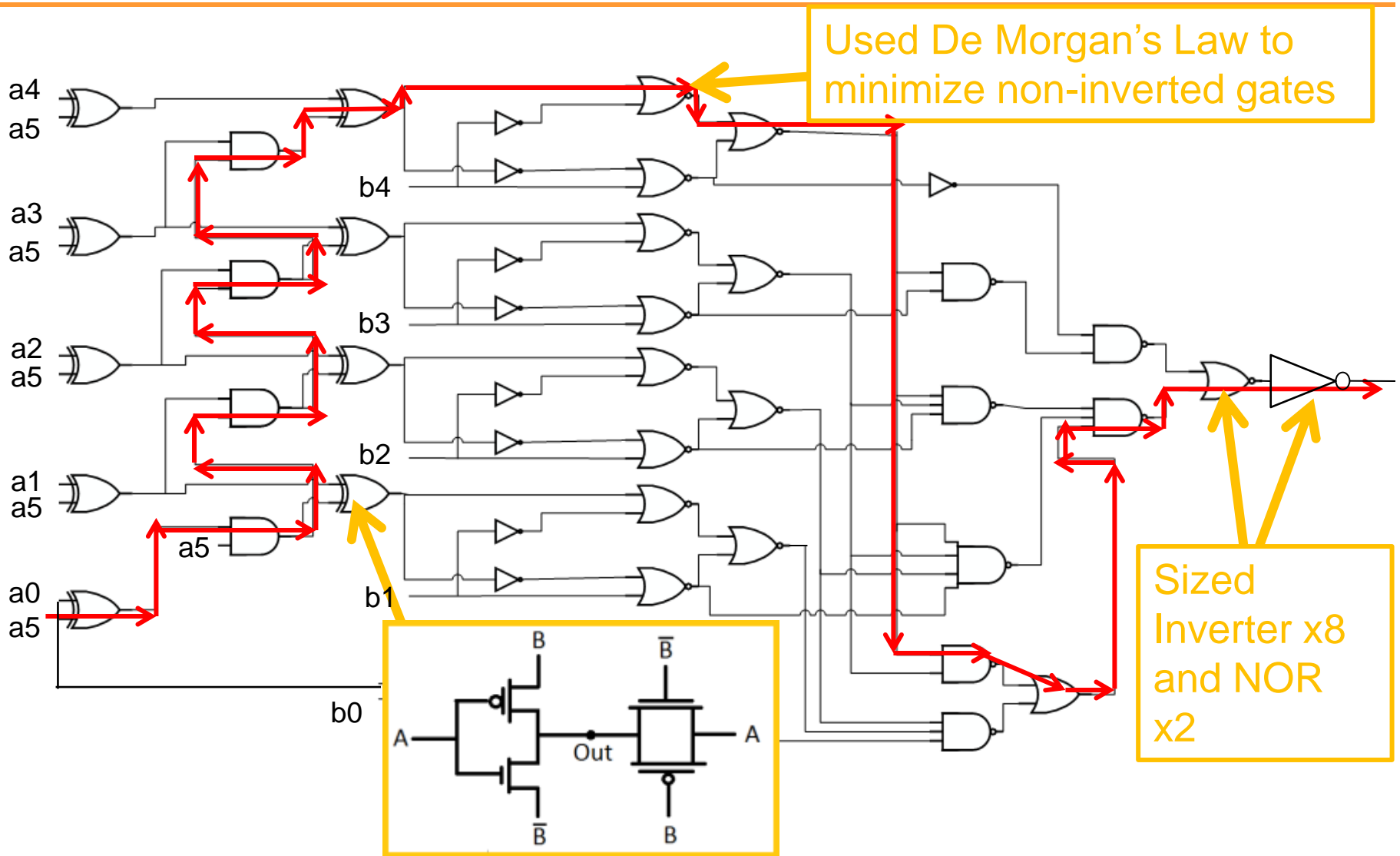
Delay	Layout size	Energy	Verification
Sch. $t_p = 999.693\text{ps}$	X= $15.77\mu\text{m}$, Y= $21.94\mu\text{m}$	Sch. E = 134.15 fJ	Func: Y
Lay. $t_p = 999.593\text{ps}$	A = $345.99\mu\text{m}^2$	Lay. E = 192.389 fJ	DRC: Y
Critical Input = $X_{5\text{ L}\rightarrow\text{H}}$	AR = 1.391	Lay. $V_{DD} =$ 629.8mV	LVS: Y

Critical Path Analysis



$$t_{\text{crit}} = t_{\text{setup}} + 5t_{\text{ripple-carry adder}} + t_{\text{1-bit comparator}} + t_{\text{Nand-Nor Logic}}$$

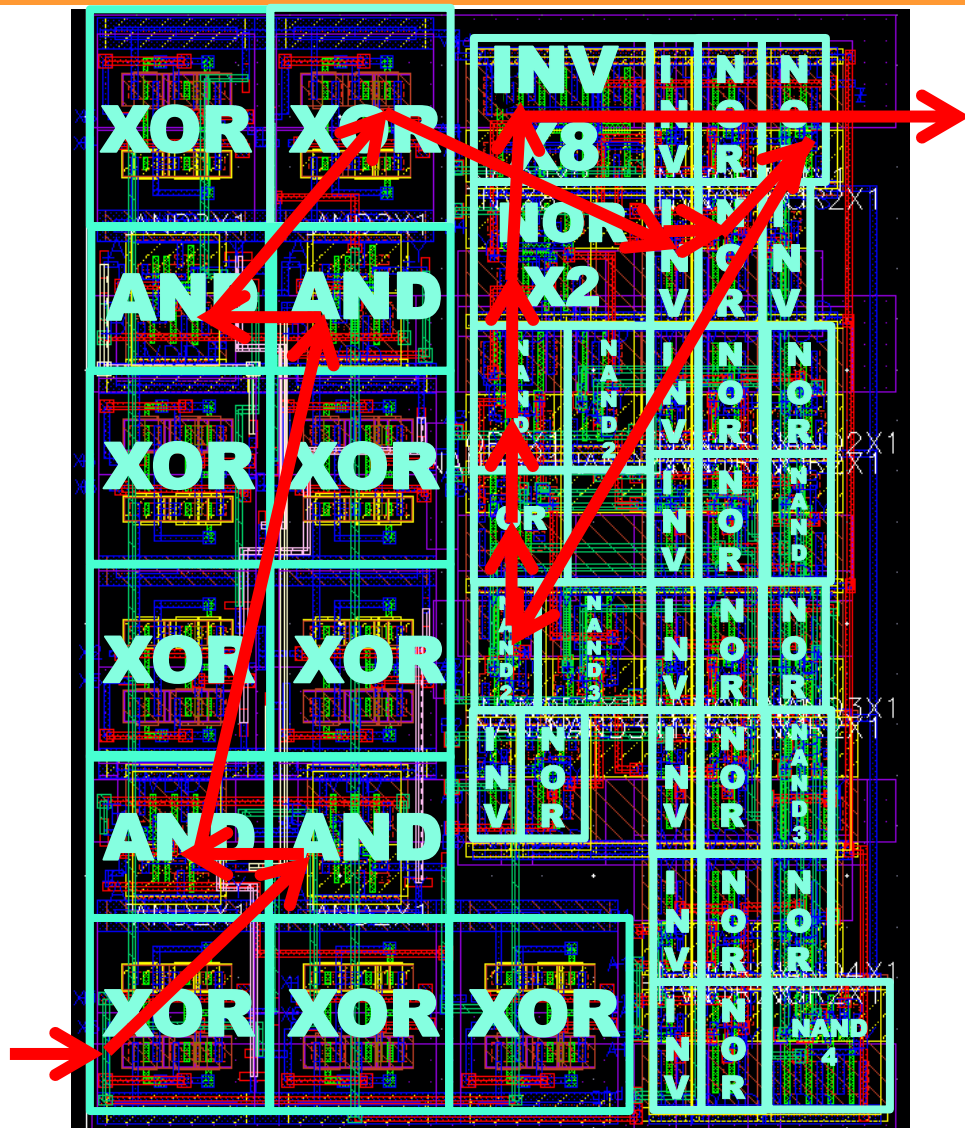
Design Optimization



Functionality Check



Absolute-Value Detector Layout



Size

$X = 15.77\mu\text{m}$

$Y = 21.94\mu\text{m}$

Aspect Ratio

1.391

Area

$345.99\mu\text{m}^2$

Density

~85%

Discussion

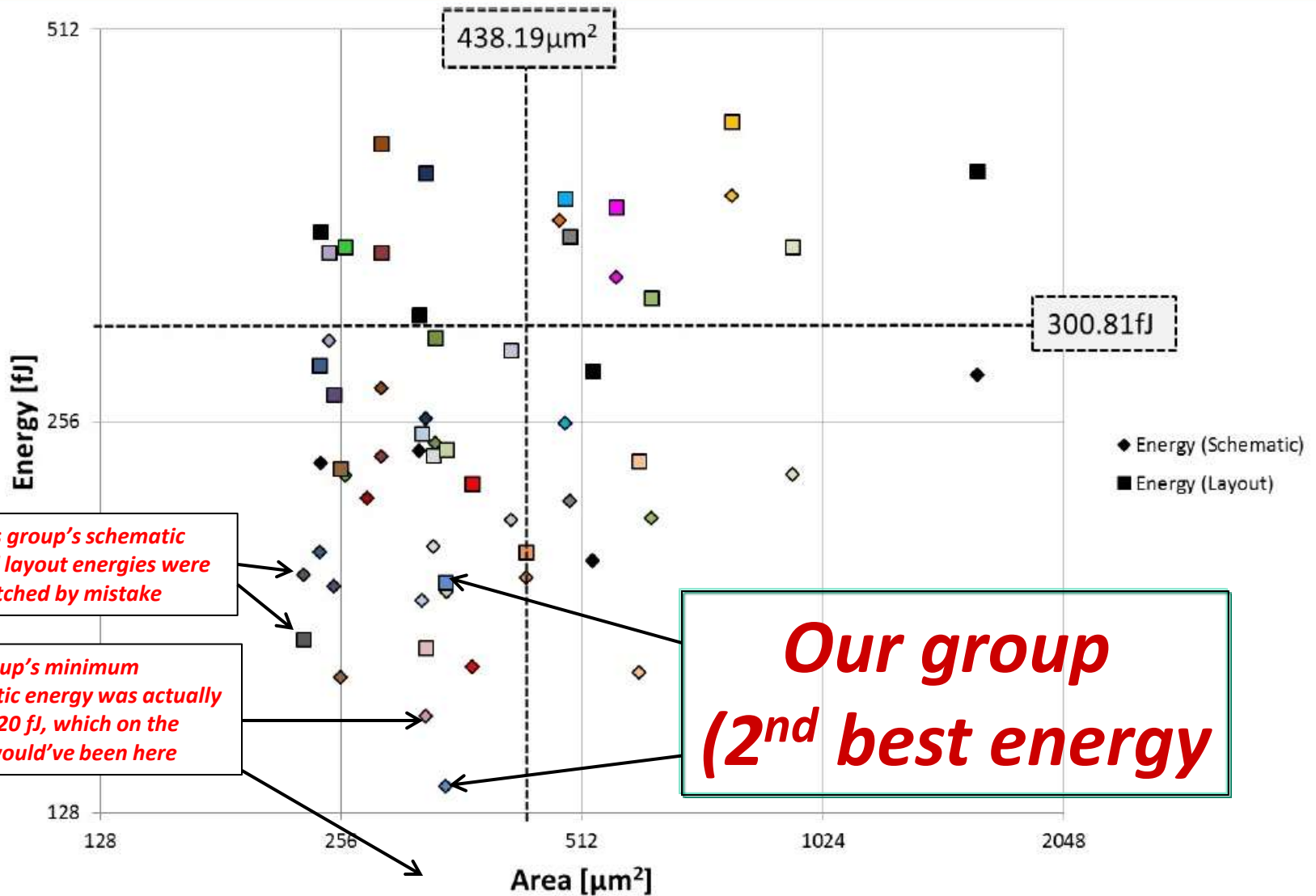
◆ Three most important features of your design

- Implemented XOR gates using transmission gates to further minimize energy
- Reduced Adder logic to use minimal gates for better efficiency
- Used De Morgan's Law throughout entire comparator to use more inverted logic gates

◆ Given another chance, 3 things you would do different

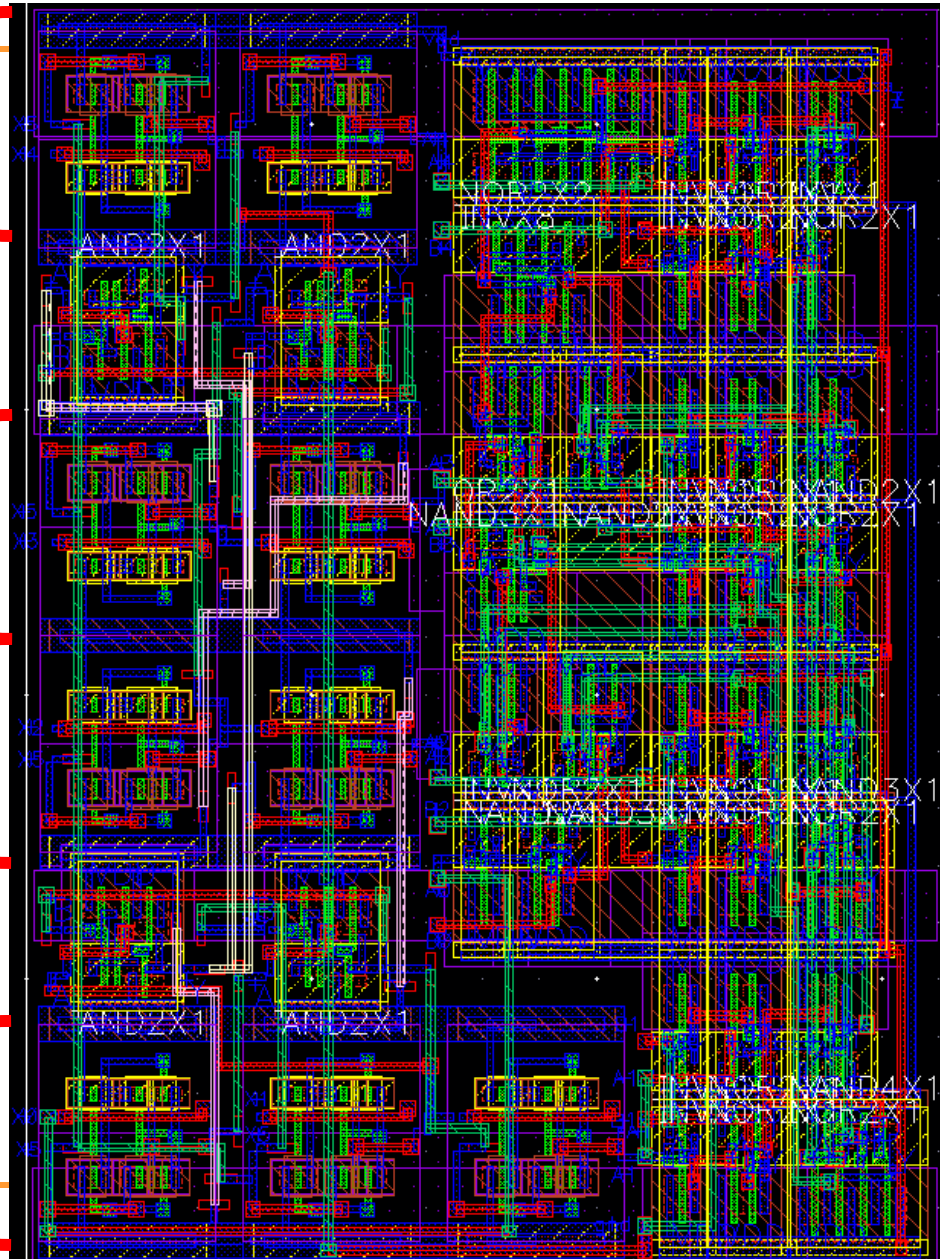
- Minimize length of critical path in layout
- Try other schematics of comparators
- Make transmission XOR layout smaller

Summary of Results: Area – Energy Space (*ln-ln* plot)



Unobstructed Layout View

I also made the layout of the transmission gate based XOR gates, on the left.



I designed the layout of the comparator, on the right half.